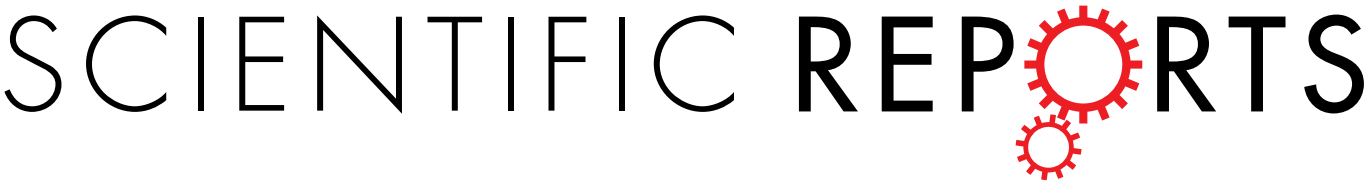

OPEN

Memristive Sisyphus circuit for clock signal generation

Yuriy V. Pershin[1,2,3], Sergey N. Shevchenko[2,4,5] & Franco Nori[2,6]

Received: 03 February 2016
Accepted: 26 April 2016
Published: 20 May 2016

Frequency generators are widely used in electronics. Here, we report the design and experimental realization of a memristive frequency generator employing a unique combination of only digital logic gates, a single-supply voltage and a realistic thresholdtype memristive device. In our circuit, the oscillator frequency and duty cycle are defined by the switching characteristics of the memristive device and external resistors. We demonstrate the circuit operation both experimentally, using a memristor emulator, and theoretically, using a model memristive device with threshold. Importantly, nanoscale realizations of memristive devices offer small-size alternatives to conventional quartz-based oscillators. In addition, the suggested approach can be used for mimicking some cyclic (Sisyphus) processes in nature, such as "dripping ants" or drops from leaky faucets.

Cyclic evolutions and relaxation oscillators are ubiquitous in nature. One example of these is the leaky faucet [Fig. 1(a)], where the suspended fluid mass increases gradually, until it suddenly decreases, when the droplet tears off[1–3]. Other examples of relaxational dynamics can also be found in granular media[4] as well as in mechanical[5] and superconducting systems[6]. Similar dynamics can be even found in wildlife. For example, some types of ants[7,8] can continuously climb a rod, aggregate, and eventually drop, right after a critical mass is accumulated [see Fig. 1(b)].

Analogous phenomena in driven dissipative systems are known as Sisyphus processes. According to Greek mythology, King Sisyphus was doomed to repeatedly push a rock uphill, which would then roll back down [Fig. 1(c)]. Recently, Sisyphus processes[9] were studied in electric circuits based on superconducting[10–13] and normal-state[14–16] systems. In these circuits, a driven artificial atom, a qubit, was coupled to either a mechanical or an electrical resonator. Depending on its detuning, the qubit was driven by the resonator either "uphill" (the usual Sisyphus process) or downhill (unusual, or "happy Sisyphus" process). The cycle was completed by relaxation to the ground state in the presence of an additional periodic signal.

Here we demonstrate a new miniaturized clock signal generator based on a memristive (memory resistive) device[17] operating in a Sisyphus-like cycle. In modern electronics, the clock signal is most frequently produced by quartz generators and sometimes by *RC*-based circuits or other approaches. The quartz generators offer a high precision at the cost of their size. Less precise *RC*-circuits are more compact. Nanoscale memristive devices[18] [combining their very small size with switching frequencies in a convenient range (e.g., hundreds of MHz)] are the core components of clock generators explored here.

In the literature, there are several known methods of using memristors in oscillating circuits. In particular, significant attention has been focused on nonlinear oscillators constructed from Chua's oscillators, by replacing Chua's diodes with memristors[19,20]. The authors of ref. 21 proposed a programmable frequency-relaxation oscillator. In such a circuit, a memristor-based digital potentiometer is used to set switching thresholds of a Schmitt trigger. Moreover, memristors can be employed to replace capacitors in relaxation oscillators resulting in compact reactance-less oscillators[22–26]. Additionally, it was shown experimentally that some polymeric memory devices exhibit slow current oscillations when subjected to a constant voltage[27]. Our work presents an advanced reactance-less oscillator design having a unique combination of only digital logic gates, a single-supply voltage and a realistic threshold-type memristive device.

In the proposed clock signal generator, the frequency is defined by the switching characteristics of a memristive device. Our circuit employs bi-polar memristive devices[18] operating in such a way that their memristances (memory resistances) increase/decrease at positive/negative voltages applied to the device, respectively. The

[1]Department of Physics and Astronomy and Smart State Center for Experimental Nanoscale Physics, University of South Carolina, Columbia, South Carolina 29208, USA. [2]CEMS, RIKEN, Saitama 351-0198, Japan. [3]Nikolaev Institute of Inorganic Chemistry SB RAS, Novosibirsk 630090, Russia. [4]B. Verkin Institute for Low Temperature Physics and Engineering, Kharkov 61103, Ukraine. [5]V. Karazin Kharkov National University, Kharkov 61022, Ukraine. [6]Physics Department, University of Michigan, Ann Arbor, Michigan 48109-1040, USA. Correspondence and requests for materials should be addressed to Y.V.P. (email: pershin@physics.sc.edu)

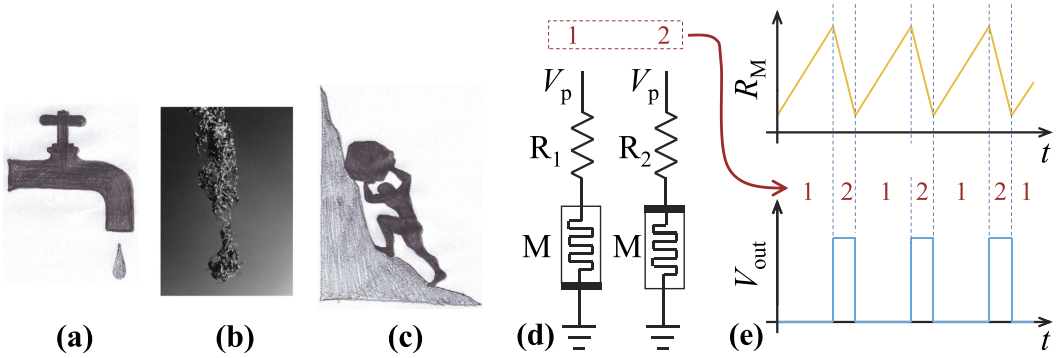

Figure 1. (**a**–**c**) Examples of Sisyphus cycles: (**a**) leaky faucet, (**b**) dripping ants[7,8], (**c**) mythological Sisyphus. (**d**) Simplified effective circuits realizing a two-phase memristive Sisyphus circuit: the increasing memristance stage 1 (left circuit) and decreasing memristance stage 2 (right circuit). Memristance oscillations and clock pulses are shown schematically on the graphs (**e**). (**b**) is reprinted with permission from ref. 7.

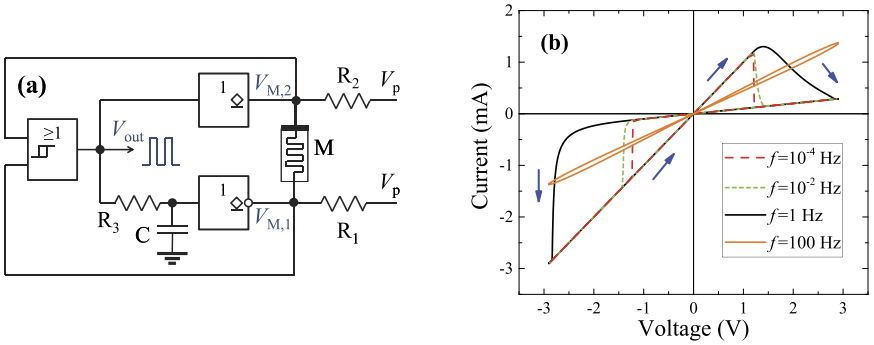

Figure 2. (**a**) A particular realization of a clock signal generator. This circuit employs an OR gate with Schmitt-trigger inputs (to the left), and open-drain identity (upper) and NOT (lower) gates. Here $V_p = 5$ V is the power supply voltage. (**b**) *I*–*V* curves of the memristive system M used in this work. The memristive system parameters are given in the text.

effective circuits depicted in Fig. 1(d) show the two stages of its operation. In stage 1 (left circuit), the positive voltage applied to the memristor M causes an increase in its memristance. In the second stage, the device polarity is changed and the memristance decreases. In this way, the memristance oscillates between two values [see Fig. 1(e)], similarly to the oscillations of the boulder height above the ground level in the Sisyphus case [Fig. 1(c)]. Importantly, the circuit does not require any large-size components (such as a quartz resonator) typically used in conventional oscillator circuits.

Memristive Clock Signal Generator

Figure 2(a) presents the specific memristive clock generator circuit introduced in this work. Its components include the memristive system M, an OR gate with Schmitt-trigger inputs (to the left), open-drain identity (upper) and NOT (lower) gates, three resistors and a capacitor. Note that the resistors R_1 and R_2 here play the same role as R_1 and R_2 in the effective circuits shown in Fig. 1(e). As will be readily observed, the output of the OR gate defines the operation stages: logical 0 corresponds to the increasing memristance stage 1, while logical 1 corresponds to the decreasing memristance stage 2. The hysteretic input levels of the Schmitt-trigger inputs (denoted by V_+ for the logic 1, and V_- for the logic 0, $V_- < V_+$) are employed as voltage thresholds triggering the stage changes. Figure 2(b) shows the calculated pinched hysteresis loops of the memristive system M described by Eqs (1–2). In this calculation, $R_M(t=0) = 2\,\text{k}\Omega$, $V_M(t) = V_0\sin(2\pi ft)$, $V_0 = 2.9$ V, and all other parameters of M are the same as in the memristor emulator specified below Eqs (1)–(2).

One can notice from Fig. 2(a) that indeed, the increasing memristance stage 1 switches to the decreasing memristance stage 2 as soon as the voltage level V_M reaches the V_+ threshold. At this instance in time, the output of the OR gate changes to 1, grounding the bottom terminal of M and setting the identity gate into the high impedance state. Assuming that $V_{M,2} > V_-$ right after the switching (below we discuss all the related requirements), the circuit will remain in the decreasing memristance stage 2 while $V_{M,2} > V_-$. The transition from stage 2 to stage 1 occurs in a similar way (as soon as $V_{M,2} < V_-$, and thus both inputs of OR become logical zeros). In Fig. 2(a), the R_3C circuit introduces a short time delay to ensure proper switching between the phases. The generator output frequency is not influenced by this delay.

Next, we discuss the experimental implementation of the clock signal generator. In our experiments, the memristive system M is realized with a digital memristor emulator[21,28]. Its main parts include a microcontroller,

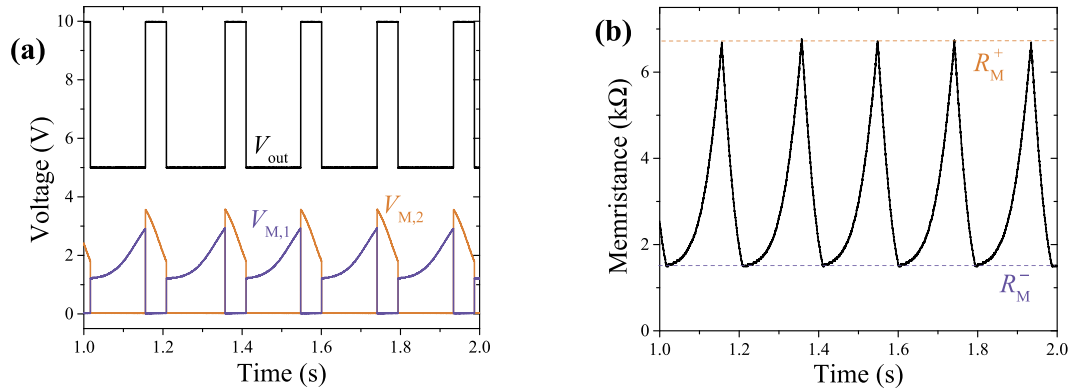

Figure 3. (**a**) Experimentally measured voltages at the output of the OR gate (V_{out}) and top and bottom electrodes of the memristive system ($V_{M,2(1)}$) in the circuit shown in Fig. 2(a). For clarity, the V_{out} is displaced by 5 V. (**b**) Memristance R_M extracted from the data presented in (**a**) by using Eq. (3).

analog-to-digital converter and digital potentiometer. The operation of the digital memristor emulator is straightforward: using the analog-to-digital converter, the microcontroller cyclically measures the voltage applied to the digital potentiometer, calculates an updated value of the memristance (using pre-programmed equations of voltage-controlled or current-controlled memristive system[17]), and writes the updated value of the memristance into the digital potentiometer. Figure 5(b) of ref. 28 presents a photograph of the specific digital memristor emulator realization employed in the present paper. More details regarding the emulator design can be found in refs 29,30.

The memristor emulator was pre-programmed with a model of voltage-controlled memristive systems with threshold[29,30]

$$I = R_M^{-1}(x)\, V_M, \tag{1}$$

$$\frac{dx}{dt} = \begin{cases} \pm\, \mathrm{sign}(V_M)\beta(|V_M| - V_t) & \text{if } |V_M| > V_t \\ 0 & \text{otherwise} \end{cases}, \tag{2}$$

where I and V_M are the current through and the voltage across the memristive system, respectively, and x is the internal state variable playing the role of the memristance. Here $R_M(x) \equiv x$, β is a positive switching constant characterizing the intrinsic rate of memristance change when $|V_M| > V_t$, V_t is the threshold voltage, and the $+$ or $-$ sign is selected according to the device connection polarity. Additionally, it is assumed that the memristance is limited to the interval $[R_{on}, R_{off}]$ (note that $R_{on} < R_{off}$). The specific model parameters used in our emulator are $\beta = 62\,\mathrm{k\Omega/V \cdot s}$, $V_t = 1.2\,\mathrm{V}$, $R_{on} = 1\,\mathrm{k\Omega}$, and $R_{off} = 10\,\mathrm{k\Omega}$, and $R_M(t=0) = (R_{on} + R_{off})/2$. We built the circuit shown in Fig. 2(b) using a TI SN74HC7032 positive-OR gate with Schmitt-trigger inputs, CD74AC05 inverters with open-drain outputs, $R_1 = 4.7\,\mathrm{k\Omega}$, $R_2 = 2.7\,\mathrm{k\Omega}$, $R_3 = 10\,\mathrm{k\Omega}$, and $C = 1.35\,\mathrm{nF}$.

Our circuit is fully reproducible within the specifications of the circuit components. Assuming that the future memristor devices will be available with well characterized characteristics (similarly, for example, to usual resistors or capacitors), we expect that the suggested circuit based on real memristors will be reproducible too. In addition, our measurements and simulations did not display any significant dispersion of the memristive properties as well of the output signal produced by the circuit. Basically, the memristor emulator operates deterministically and thus the circuit also operates deterministically. As deterministic models are frequently used to describe the response of real memristive devices and, in many cases, show a very good agreement with experiments, we believe that the selected approach (based on the emulator) illustrates our idea in a very realistic manner.

Figure 3(a) presents results of our measurements. While the $V_{M,1}$ and $V_{M,2}$ curves clearly demonstrate two stages of the circuit operation, the output V_{out} [displayed in Fig. 2(a)] shows a stable clock signal with a period of about 0.194 s and a duty cycle of about 27%. With the knowledge of R_1 and R_2, the $V_{M,1}$ and $V_{M,2}$ curves were used to extract the time dependence of the memristance R_M depicted in Fig. 3(b). Its variations are similar to the desired variations of R_M sketched in Fig. 1(e).

Circuit Analysis

In Fig. 3(b), the memristance R_M of M changes periodically from R_M^- to R_M^+, and back (see also Fig. 1(e)). Analytically, one can find the corresponding durations of the time intervals, τ_1 and τ_2. In what follows, we focus on the effective circuit models depicted in Fig. 2(d) to find τ_1 and τ_2 analytically.

For the sake of convenience, let us consider the system dynamics from $t = 0$ in both stages and perform calculations based on the memristive device model employed in our emulator [Eqs (1, 2)]. Then, using

$$V_{M,i}(t) = V_p \frac{R_{M,i}(t)}{R_i + R_{M,i}(t)}, \tag{3}$$

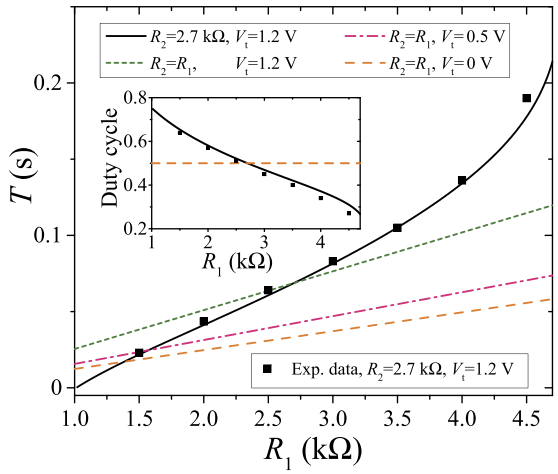

Figure 4. Period $T=\tau_1+\tau_2$ as function of the resistance R_1. Inset: the duty cycle τ_2/T as a function of R_1. This plot was obtained using the following set of parameters: $V_p=5$ V, $V_+=3$ V, $V_-=1.8$ V, and $\beta=62$ kΩ/V · s. Note that R_2 and V_t are indicated on the plot.

where $i=1, 2$ denotes the two time intervals, we integrate Eq. (2) with appropriate initial and final conditions for both intervals, and accounting for the memristor polarity. As a result, one can find the following expression for the duration of the two stages

$$\tau_i = \frac{1}{\beta}\frac{R_M^+ - R_M^-}{V_p - V_t} + \frac{1}{\beta}\frac{R_i V_p}{(V_p - V_t)^2}\ln\left\{\frac{(V_p - V_t)R_M^+ - V_t R_i}{(V_p - V_t)R_M^- - V_t R_i}\right\}. \tag{4}$$

The oscillation period is given by

$$T = \tau_1 + \tau_2. \tag{5}$$

The boundary values of the memristance, R_M^- and R_M^+, can be expressed through the Schmitt-trigger input thresholds as

$$R_M^+ = \frac{R_1 V_+}{V_p - V_+}, \quad R_M^- = \frac{R_2 V_-}{V_p - V_-}. \tag{6}$$

The expression for the period T can be written in a simple form assuming that $R_1=R_2$ and $V_p \gg V_t$ (and also $R_1 \lesssim R_M^-$ so that $V_p R_M^- \gg V_t R_1$). Then we obtain

$$T = \frac{2}{\beta}\frac{R_1}{V_p}\left\{\frac{R_M^+ - R_M^-}{R_1} + \ln\frac{R_M^+}{R_M^-}\right\}. \tag{7}$$

This together with Eq. (6) gives

$$T = \frac{2}{\beta}\frac{R_1}{V_p}\left\{\frac{V_p(V_+ - V_-)}{(V_p - V_+)(V_p - V_-)} + \ln\frac{V_+(V_p - V_-)}{V_-(V_p - V_+)}\right\}. \tag{8}$$

The above formulas are plotted in Fig. 4. There, it is assumed that all the circuit parameters (except R_1 and R_2) are fixed. This figure shows that both the period T and the duty cycle τ_2/T can be tuned in a certain range by varying R_1 and/or R_2. In Fig. 4, the solid curve was plotted for the same value of R_2 as used in the experiment, while the other curves demonstrate the changes assuming equal resistances, $R_2=R_1$, for several values of the memristor threshold voltage V_t. In particular, Fig. 4 demonstrates that the formula (8), which is valid at $V_t=0$ and $R_2=R_1$, provides a good estimation for the period T for small values of the threshold voltage V_t when $R_2=R_1$. Moreover, Fig. 4 also shows several experimentally measured periods and corresponding duty cycles that exhibit a very good agreement with our analytical results.

Finally, we consider the limitations imposed on the clock signal generator components required for its proper operation. The numerical estimations provided below employ parameter values that are close to those of our experimental implementation of the signal generator. For the convenience of readers, here we list the values of these parameters: $V_p=5$ V, $V_+=3$ V, $V_-=1.8$ V, $V_t=1.2$ V, $R_{on}=1$ kΩ, and $R_{off}=10$ kΩ.

1. In the stage 1, the minimum (maximum) values of V_M must be below (above) V_+; namely, $V_M(R_{on}) < V_+$ and $V_M(R_{off}) > V_+$. Consequently,

$$R_{on}\frac{(V_p - V_+)}{V_+} < R_1 < R_{off}\frac{(V_p - V_+)}{V_+}. \quad (9)$$

Numerically, $0.667\,k\Omega < R_1 < 6.67\,k\Omega$.

2. In the stage 2, the minimum (maximum) values of V_M must be below (above) V_-, namely, $V_M(R_{on}) < V_-$ and $V_M(R_{off}) > V_-$. Consequently,

$$R_{on}\frac{(V_p - V_-)}{V_-} < R_2 < R_{off}\frac{(V_p - V_-)}{V_-}. \quad (10)$$

Numerically, $1.778\,k\Omega < R_2 < 17.78\,k\Omega$.

3. Moreover, right after the switching from stage 1 to stage 2, the voltage across M should stay above V_-, namely, $V_- < V_p R_M^+/(R_M^+ + R_2)$, where R_M^+ is given by Eq. (6). It follows that

$$\frac{R_2}{R_1} < \frac{V_+(V_p - V_-)}{V_-(V_p - V_+)} \quad (11)$$

and, numerically, $R_2/R_1 < 2.67$. We note that the requirement that in the transition from stage 2 to stage 1 the voltage across M stays below V_+, is also given by Eq. (11). For the same transition, one can also require that $V_M(R_M^-) > V_t$ in stage 1, however, this requirement is weaker than the criterion 4.

4. In order to start oscillations from *any* initial condition, the voltage across M (in the worst-case limit $R_M = R_{on}$) should exceed V_t. This results in

$$R_1 < R_{on}\left(\frac{V_p}{V_t} - 1\right). \quad (12)$$

Using the above-mentioned parameters, we obtain $R_1 < 3.167\,k\Omega$.

5. Lastly, we mention the obvious requirement on V_-, namely, $V_t < V_-$.

One can easily notice that in our experimental implementation of the circuit shown in Fig. 2(b), the selected values of $R_1 = 4.7\,k\Omega$ and $R_2 = 2.7\,k\Omega$ satisfy the criteria in Eqs (9–11). Regarding the criterion (12), we were able to use a large value of R_1, because the initial value of the emulator memristance was selected above R_{on}.

Conclusion

We have proposed and analyzed the design of a memristive clock signal generator. Assuming a realistic threshold model of a memristive device, we experimentally demonstrated the operation of a memristive frequency generator. While our demonstration is based on a slow memristor emulator, the real memristive devices can result in frequencies in the industrially important MHz-GHz range. Moreover, the specific proposed circuit for frequency generation offers frequency and duty cycle tunability. These theoretical considerations together with our experimental emulation shows the potential of such circuits for very compact frequency generators.

References

1. Utada, A. S., Fernandez-Nieves, A., Stone, H. A. & Weitz, D. A. Dripping to jetting transitions in coflowing liquid streams. *Phys. Rev. Lett.* **99,** 094502 (2007).
2. Ambravaneswaran, B., Phillips, S. D. & Basaran, O. A. Theoretical analysis of a dripping faucet. *Phys. Rev. Lett.* **85,** 5332 (2000).
3. Plourde, B., Nori, F. & Bretz, M. Water droplet avalanches. *Phys. Rev. Lett.* **71,** 2749–2752 (1993).
4. Benza, V. G., Nori, F. & Pla, O. Mean-field theory of sandpile avalanches: From the intermittent- to the continuous-flow regime. *Phys. Rev. E* **48,** 4095–4098 (1993).
5. Field, S., Venturi, N. & Nori, F. Marginal stability and chaos in coupled faults modeled by nonlinear circuits. *Phys. Rev. Lett.* **74,** 74–77 (1995).
6. Field, S., Witt, J., Nori, F. & Ling, X. Superconducting vortex avalanches. *Phys. Rev. Lett.* **74,** 1206–1209 (1995).
7. Bonabeau, E. *et al.* Dripping faucet with ants. *Phys. Rev. E* **57,** 5904–5907 (1998).
8. Theraulaz, G. *et al.* Model of droplet dynamics in the argentine ant linepithema humile (mayr). *Bulletin of Mathematical Biology* **63,** 1079–1093 (2001).
9. Cohen-Tannoudji, C. & Phillips, W. D. New mechanisms for laser cooling. *Phys. Today* **43,** 33–40 (1990).
10. Grajcar, M. *et al.* Sisyphus cooling and amplification by a superconducting qubit. *Nature Phys.* **4,** 612–616 (2008).
11. Nori, F. Superconducting qubits: Atomic physics with a circuit. *Nature Phys.* **4,** 589–590 (2008).
12. Skinner, J. C., Prance, H., Stiffell, P. B. & Prance, R. J. Sisyphus effects in a microwave-excited flux-qubit resonator system. *Phys. Rev. Lett.* **105,** 257002 (2010).
13. Persson, F., Wilson, C. M., Sandberg, M., Johansson, G. & Delsing, P. Excess dissipation in a single-electron box: The Sisyphus resistance. *Nano Lett.* **10,** 953–957 (2010).
14. Gonzalez-Zalba, M. F., Barraud, S., Ferguson, A. J. & Betz, A. C. Probing the limits of gate-based charge sensing. *Nature Comm.* **6,** 6084 (2015).
15. Shevchenko, S. N., Rubanov, D. G. & Nori, F. Delayed-response quantum back action in nanoelectromechanical systems. *Phys. Rev. B* **91,** 165422 (2015).
16. Gullans, M. J. *et al.* Sisyphus thermalization of photons in a double quantum dot. *arXiv:1512.01248* (2015).
17. Chua, L. O. & Kang, S. M. Memristive devices and systems. *Proc. IEEE* **64,** 209–223 (1976).
18. Pershin, Y. V. & Di Ventra, M. Memory effects in complex materials and nanoscale systems. *Advances in Physics* **60,** 145–227 (2011).
19. Itoh, M. & Chua, L. O. Memristor oscillators. *Int. J. Bif. Chaos* **18,** 3183–3206 (2008).
20. Corinto, F., Ascoli, A. & Gilli, M. Nonlinear dynamics of memristor oscillators. *IEEE Trans. Circ. Syst. I* **58,** 1323 (2011).
21. Pershin, Y. V. & Di Ventra, M. Practical approach to programmable analog circuits with memristors. *IEEE Trans. Circ. Syst. I* **57,** 1857 (2010).
22. Zidan, M. A., Omran, H., Radwan, A. G. & Salama, K. N. Memristor-based reactance-less oscillator. *El. Lett.* **47,** 1220 (2011).

23. Mosad, A., Fouda, M., Khatib, M., Salama, K. & Radwan, A. Improved memristor-based relaxation oscillator. *Microelectronics Journal* **44,** 814 (2013).
24. Yu, D., Iu, H. H. C., Fitch, A. L. & Liang, Y. A floating memristor emulator based relaxation oscillator. *IEEE Trans. Circ. Syst. I* **61,** 2888 (2014).
25. Zidan, M. A. *et al.* A family of memristor-based reactance-less oscillators. *International Journal of Circuit Theory and Applications* **42,** 1103 (2014).
26. Kyriakides, E. & Georgiou, J. A compact, low-frequency, memristor-based oscillator. *International Journal of Circuit Theory and Applications* **43,** 1801 (2015).
27. Erokhin, V., Berzina, T., Camorani, P. & Fontana, M. P. Non-equilibrium electrical behaviour of polymeric electrochemical junctions. *Journal of Physics: Condensed Matter* **19,** 205111 (2007).
28. Pershin, Y. V. & Di Ventra, M. Teaching memory circuit elements via experiment-based learning. *IEEE Circ. Syst. Mag.* **12,** 64–74 (2012).
29. Pershin, Y. V., Slipko, V. A. & Di Ventra, M. Complex dynamics and scale invariance of one-dimensional memristive networks. *Phys. Rev. E* **87,** 022116 (2013).
30. Pershin, Y. V., La Fontaine, S. & Di Ventra, M. Memristive model of amoeba learning. *Phys. Rev. E* **80,** 021926 (2009).

Acknowledgements

This work has been supported by the NSF grant No. ECCS-1202383, USC Smart State Center for Experimental Nanoscale Physics, the RIKEN iTHES Project, MURI Center for Dynamic Magneto-Optics, and a Grant-in-Aid for Scientific Research (A), and Russian Scientific Foundation grant No. 15-13-20021.

Author Contributions

Y.V.P. conducted the experiment, Y.V.P. and S.N.S. did the calculations. All the authors discussed the results and co-wrote the manuscript.

Additional Information

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Pershin, Y. V. *et al.* Memristive Sisyphus circuit for clock signal generation. *Sci. Rep.* **6**, 26155; doi: 10.1038/srep26155 (2016).